

Figure 2
Prior Art

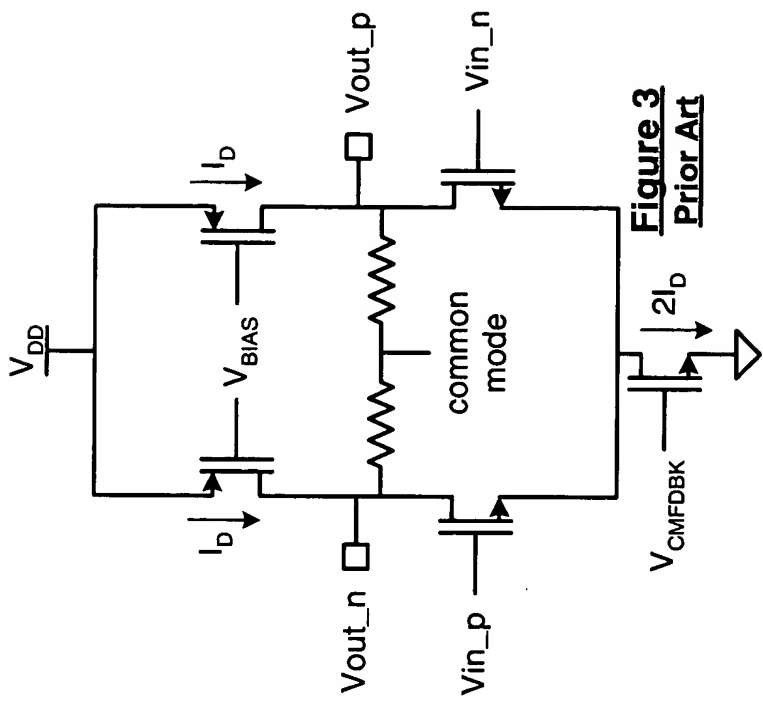


Figure 3
Prior Art

----- $V_{DD} = 3.3 \text{ V}$

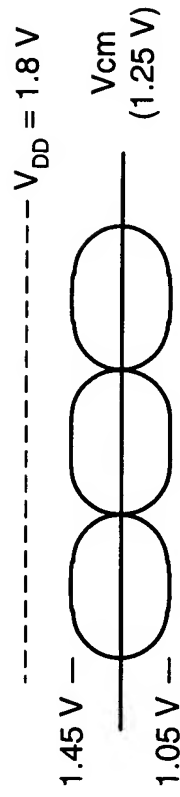


Figure 1
Prior Art

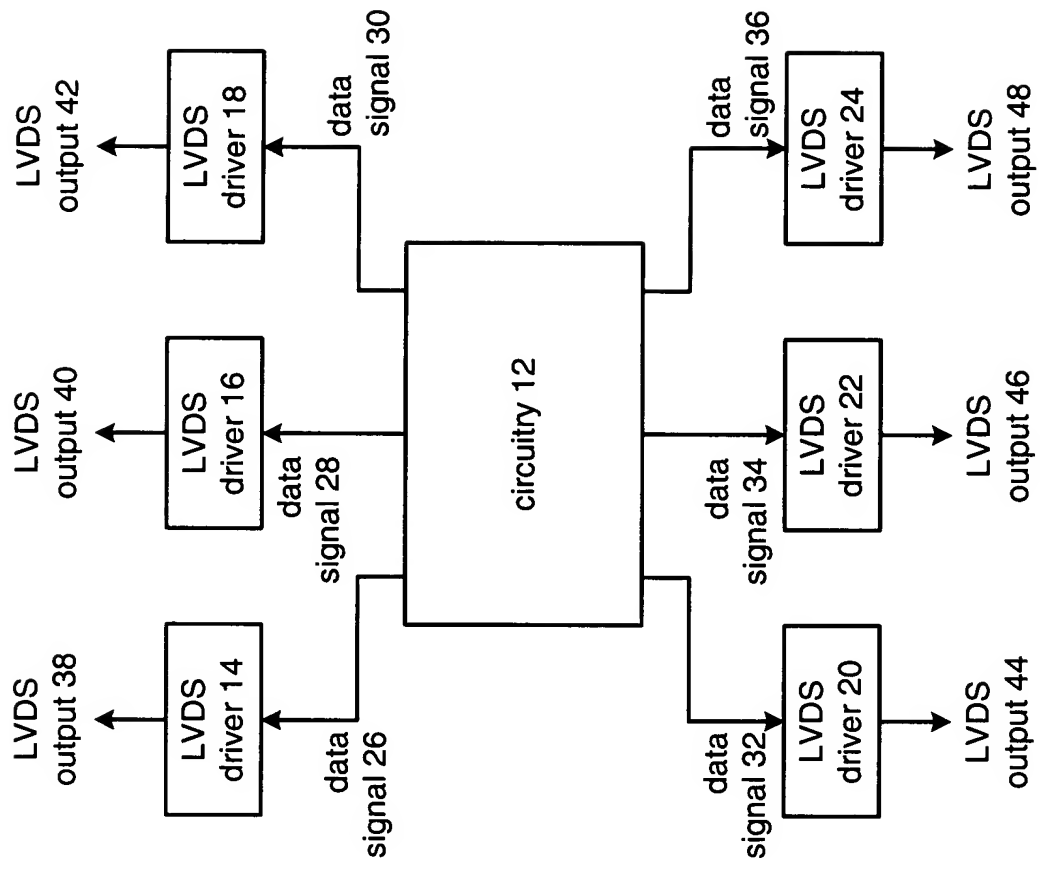


Figure 4
integrated circuit 10

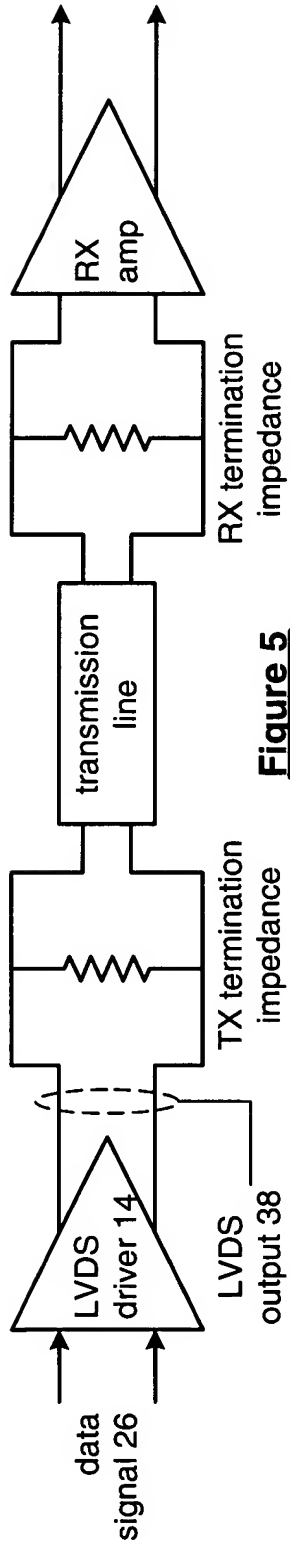


Figure 5

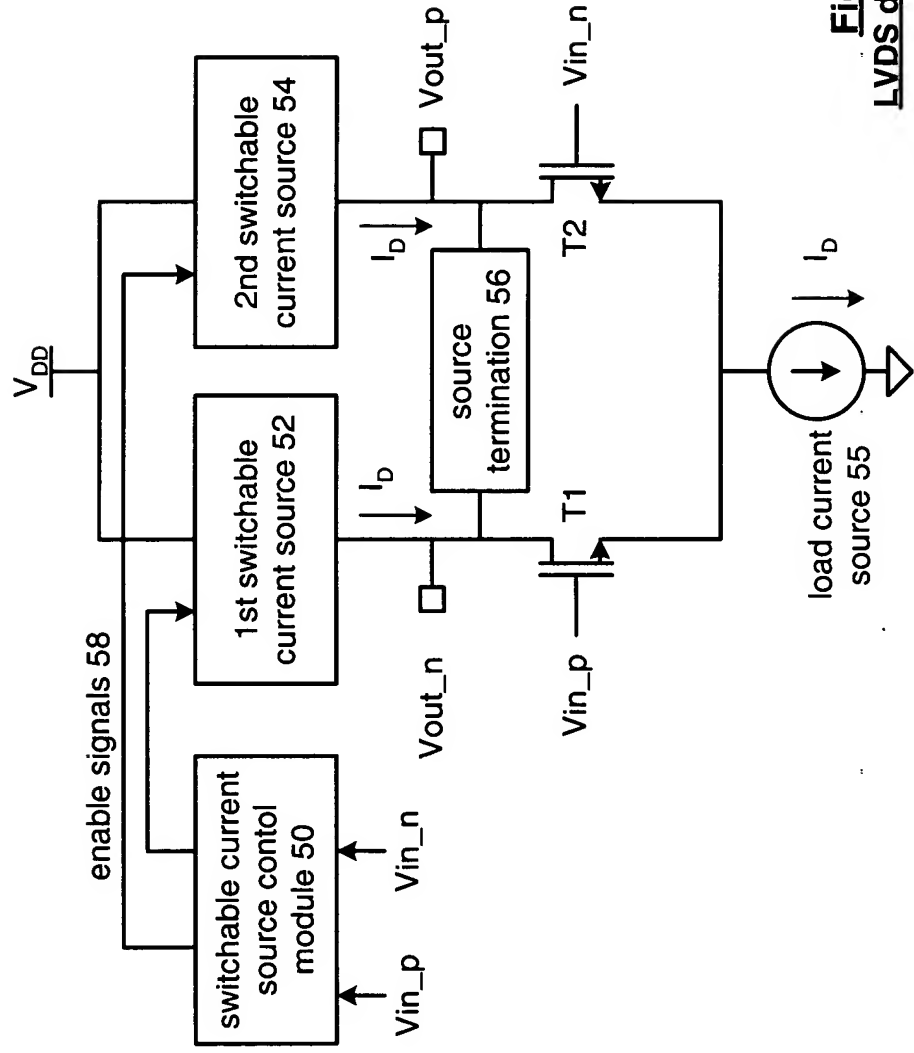


Figure 6
LVDS driver 14 - 24

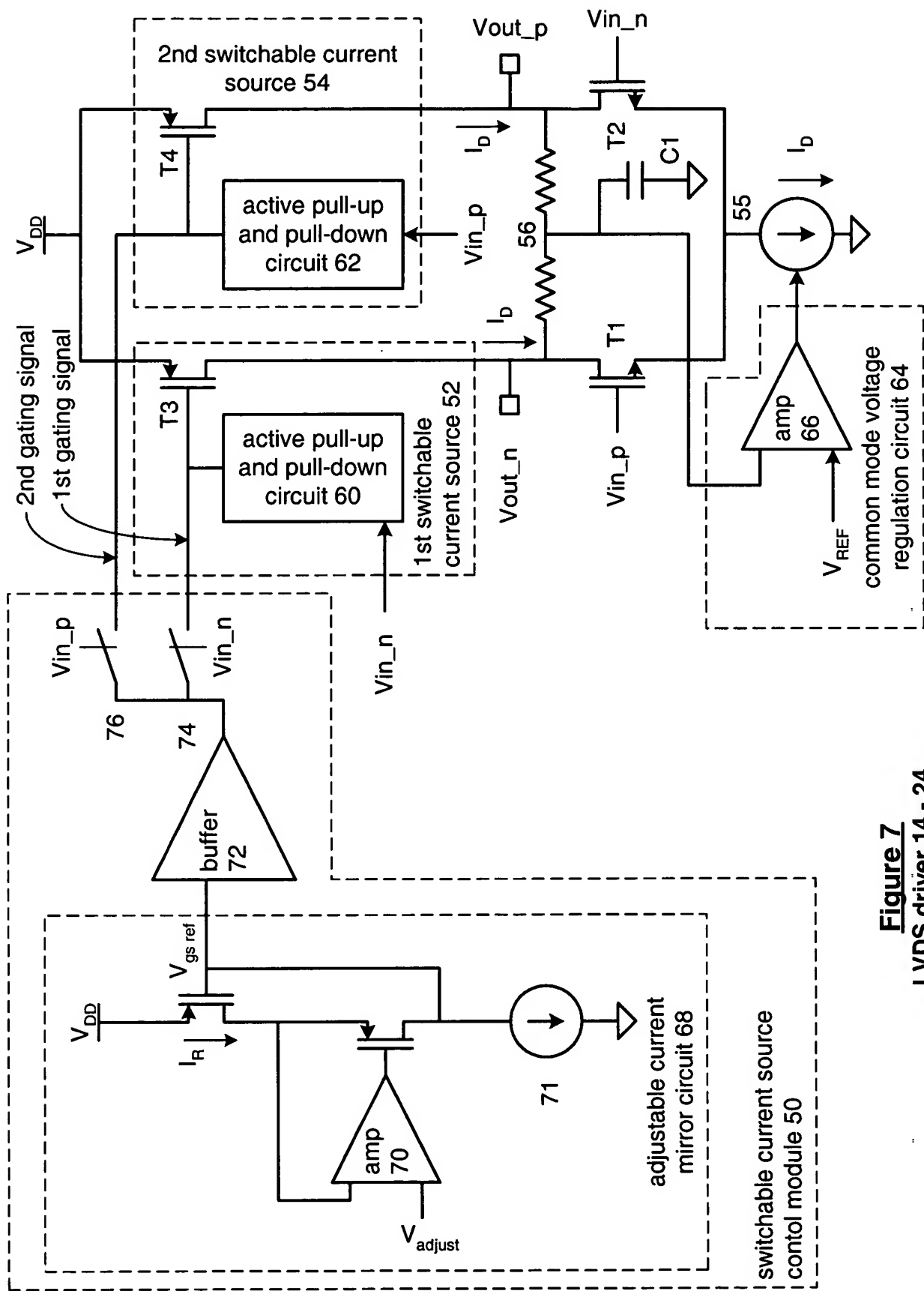


Figure 7
LVDS driver 14 - 24

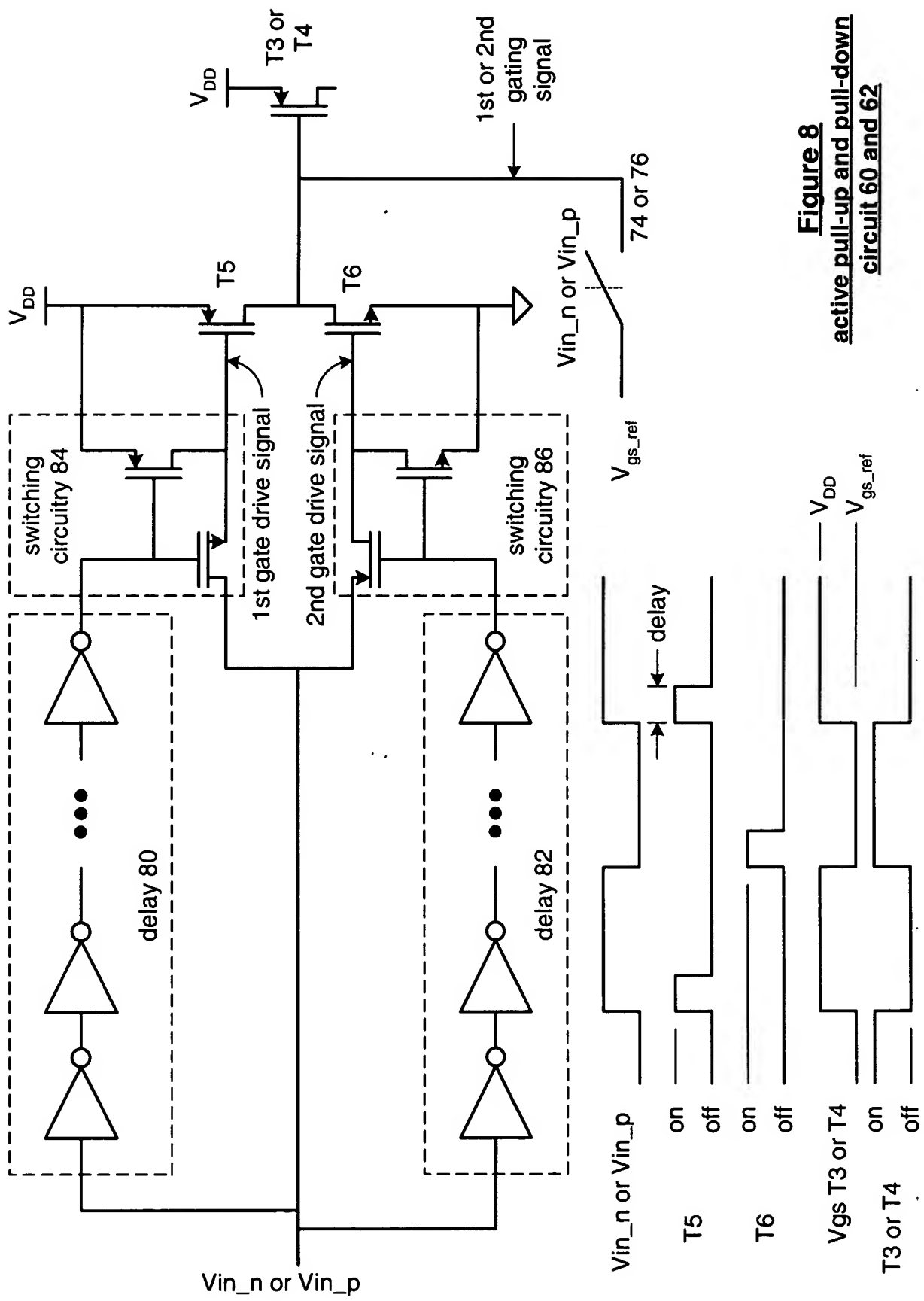


Figure 8
active pull-up and pull-down
circuit 60 and 62

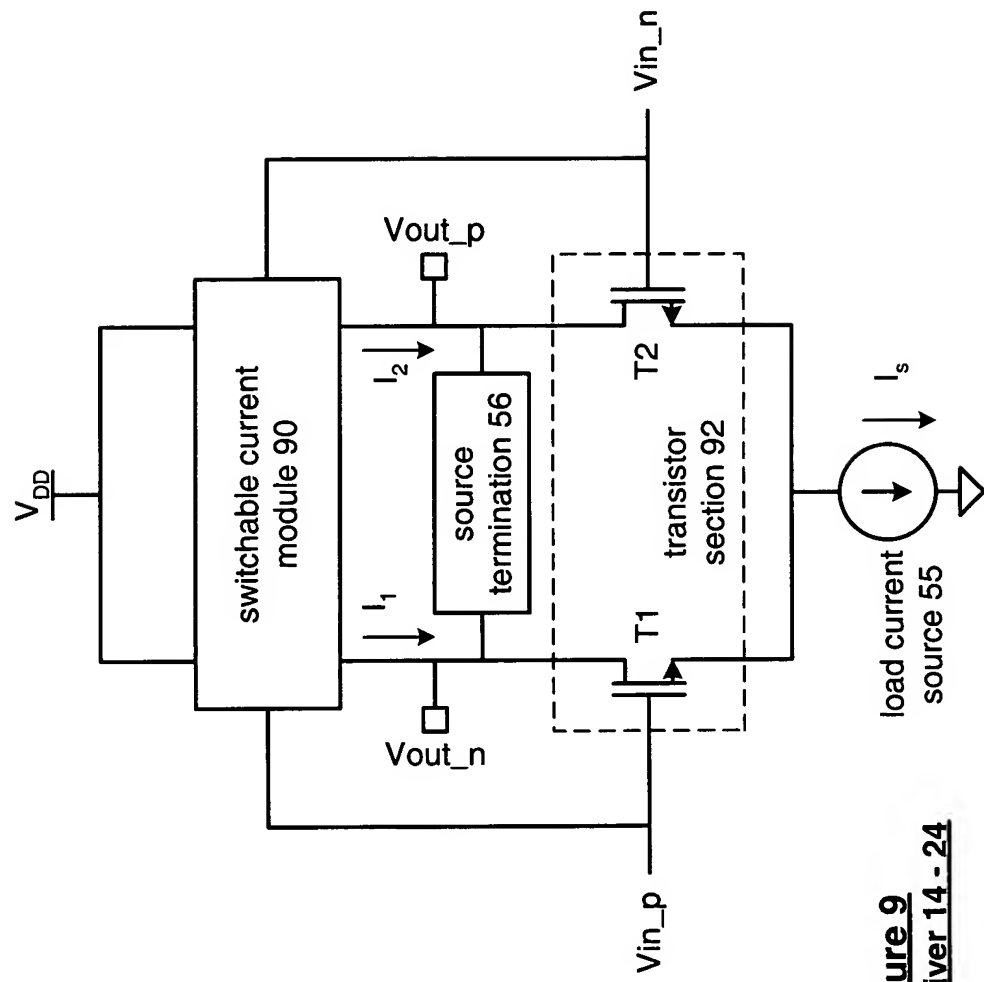


Figure 9
LVDS driver 14 - 24

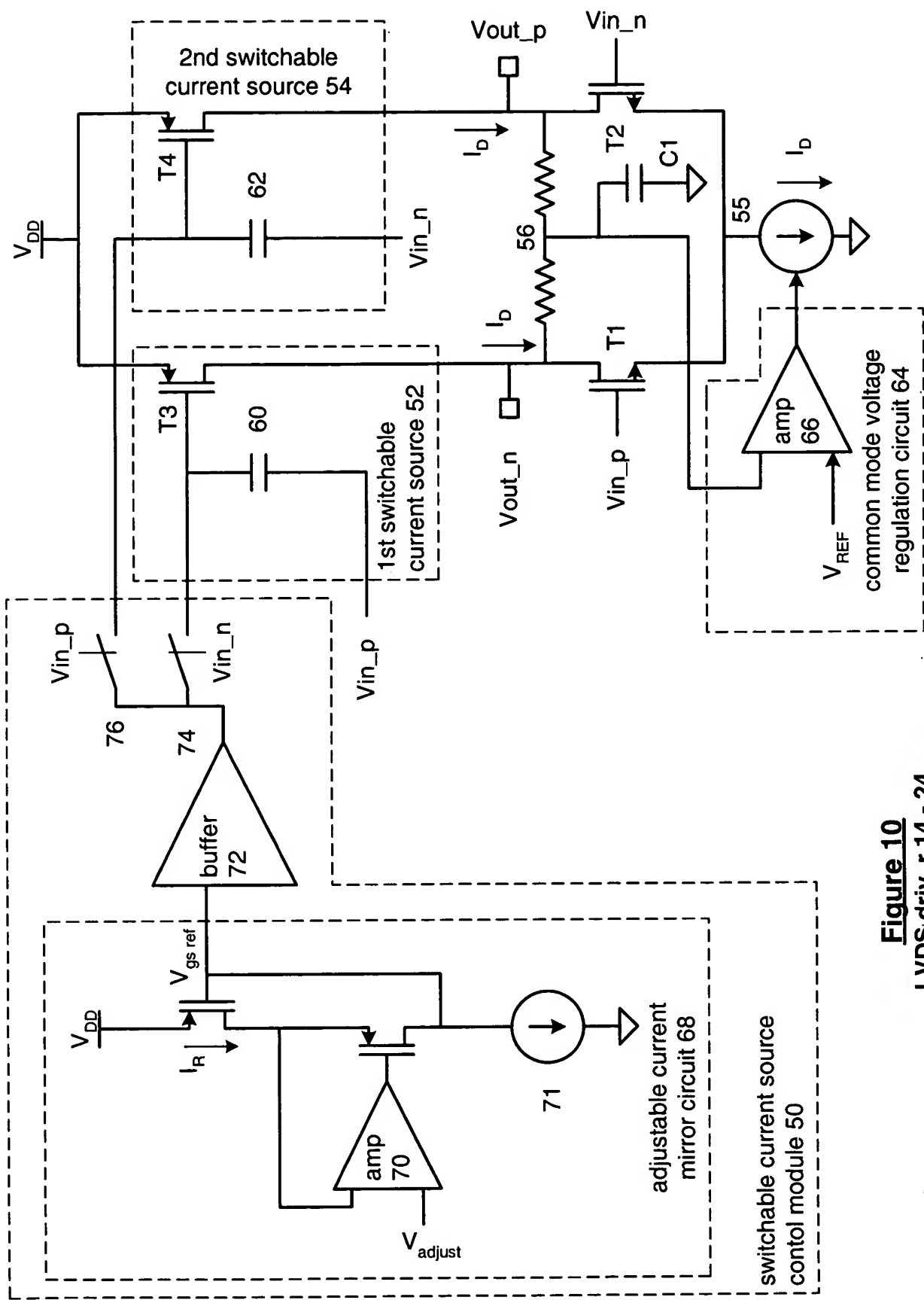


Figure 10
LVDS driv r 14 - 24